

WHAT IS CLAIMED IS:

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1. A semiconductor device comprising:  
a plurality of function blocks;  
a plurality of buses, each of which is  
respectively connected to one of the plurality of  
10 function blocks;  
a plurality of control signal lines, each  
of which is respectively connected to one of the  
plurality of function blocks;  
a main bus;  
15 a bus control unit connected to the main  
bus;  
a bus division control unit located  
between the plurality of buses and the main bus, for  
connecting one of the plurality of buses to the main  
20 bus and transmitting a control signal to a  
corresponding one of the plurality of control signal  
lines in accordance with a decoded result of  
information supplied from the bus control unit via  
the main bus, thereby controlling a corresponding  
25 one of the plurality of function blocks.

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2. The semiconductor device as claimed in  
claim 1, wherein the bus division control unit  
comprises:  
a decoder unit for decoding the  
information supplied from the bus control unit via  
35 the main bus and generating the control signal; and  
a bus dividing unit for connecting one of  
the plurality of buses to the main bus, in

accordance with a decoded result of the decoder unit.

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3. The semiconductor device as claimed in claim 1, wherein the bus division control unit connects one of the plurality of buses to the main bus, in accordance with a decoded result of address information transmitted from the bus control unit via the main bus.

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4. The semiconductor device as claimed in claim 1, wherein

at least two of the plurality of function blocks shares one of the plurality of buses, and

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the bus division control unit controls a transfer operation between the two function blocks via the one of the plurality of buses in response to a transfer request signal.

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5. The semiconductor device as claimed in claim 4, wherein the bus division control unit simultaneously transmits a write-enable signal to one of the two function blocks and a read-enable signal to the other one of the two function blocks.

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6. The semiconductor device as claimed in

claim 4, wherein the bus division control unit receives a transfer control signal and determines a transfer source and a transfer destination between the two function blocks in accordance with the transfer control signal.

10           7. The semiconductor device as claimed in claim 4, wherein, when an access request to one of the two function blocks is made by the bus control unit, the bus division control unit processes the access request prior to processing the transfer request.

20           8. The semiconductor device as claimed in claim 4, wherein, when an access request to one of the plurality of function blocks other than the two function blocks is made by the bus control unit, the bus division control unit processes the access request in parallel with processing the transfer request.

30           9. The semiconductor device as claimed in claim 1, wherein the bus division control unit determines whether an access made by the bus control unit is a read access or a write access based on a decoded result of information supplied from the bus control unit via the main bus, and connects one of the plurality of buses to the main bus in the access

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10. A semiconductor device comprising:  
a plurality of buses;  
10 a main bus; and  
a bus division control unit located  
between the plurality of buses and the main bus, for  
connecting a first bus of the plurality of buses to  
the main bus in accordance with a decoded result of  
15 information on the main bus, and controlling a  
transferring operation between two function blocks  
connected to a second bus of the plurality of buses.